

Description

The Atmel® | SMART™ SAM D10 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 14- to 24-pins with up to 16KB Flash and 4KB of SRAM. The SAM D10 devices operate at a maximum frequency of 48MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces. The SAM D10 series is compatible to the other product series in the SAM D family, enabling easy migration to larger device with added features.

The Atmel SAM D10 devices provide the following features: In-system programmable Flash, six-channel direct memory access (DMA) controller, 6 channel Event System, programmable interrupt controller, up to 22 programmable I/O pins, 32-bit real-time clock and calendar, two 16-bit Timer/Counters (TC) and one 24-bit Timer/Counter for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and one timer/counter has extended functions optimized for motor, lighting and other control applications. The series provide up to three Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 3.4MHz, SMBus, PMBus and LIN slave; up to 10-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 72 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D10 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug and trace of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM D10 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Features

- Processor
 - ARM Cortex-M0+ CPU running at up to 48MHz
 - Single-cycle hardware multiplier
 - Micro Trace Buffer
- Memories
 - 8/16KB in-system self-programmable Flash
 - 4KB SRAM Memory
- System
 - Power-on reset (POR) and brown-out detection (BOD)
 - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
 - External Interrupt Controller (EIC)
 - 8 external interrupts
 - One non-maskable interrupt
 - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
 - Idle and standby sleep modes
 - SleepWalking peripherals
- Peripherals
 - 6-channel Direct Memory Access Controller (DMAC)
 - 6-channel Event System
 - Two 16-bit Timer/Counters (TC), configurable as either:
 - One 16-bit TC with compare/capture channels
 - One 8-bit TC with compare/capture channels
 - One 32-bit TC with compare/capture channels, by using two TCs
 - One 24-bit Timer/Counters for Control (TCC), with extended functions:
 - Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
 - 32-bit Real Time Counter (RTC) with clock/calendar function
 - Watchdog Timer (WDT)
 - CRC-32 generator
 - Up to three Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C Bus up to 3.4MHz
 - SMBUS/PMBUS
 - SPI
 - LIN slave
 - 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 10 channels
 - Differential and single-ended input
 - 1/2x to 16x programmable gain stage
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
 - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
 - Two Analog Comparators (AC) with window compare function
 - Peripheral Touch Controller (PTC)
 - Up to 72-channel capacitive touch and proximity sensing
- I/O
 - Up to 22 programmable I/O pins
- Packages
 - 24-pin QFN
 - 20-pin SOIC
 - 20-ball WLCSP
 - 14-pin SOIC
- Operating Voltage
 - 1.62V – 3.63V

1. Configuration Summary

Table 1-1. Configuration Summary

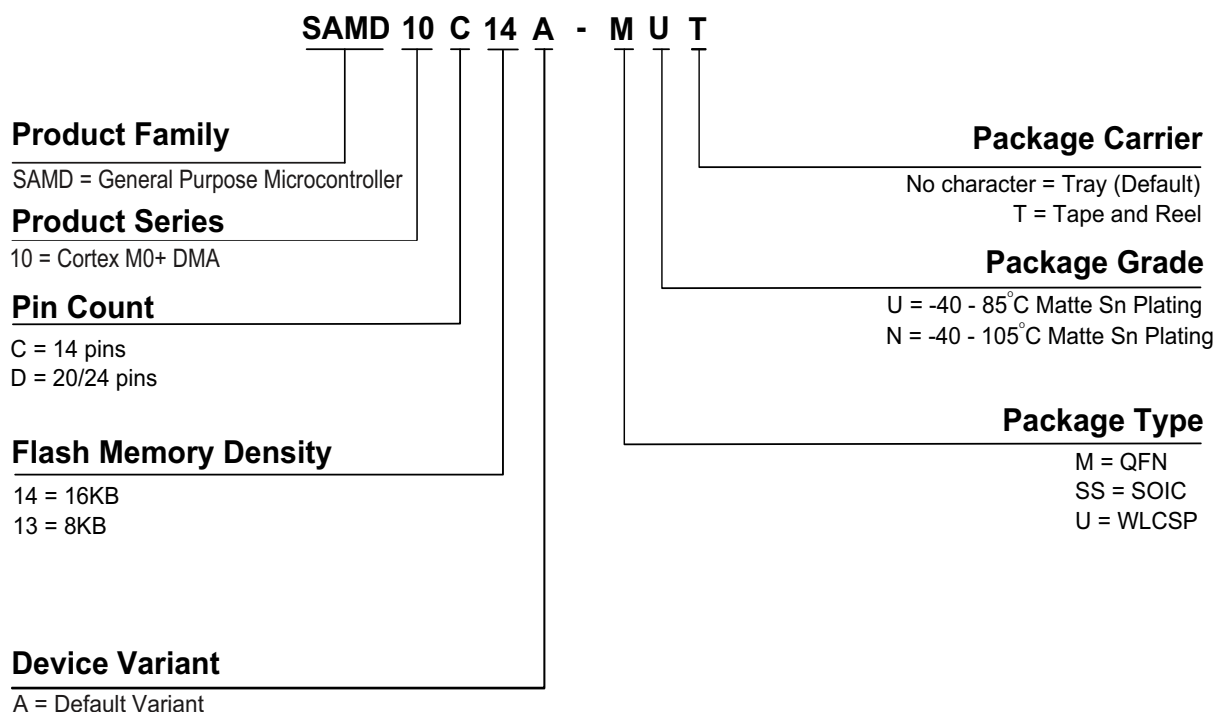
	SAM D10D – 24-pin QFN	SAM D10D – 20-pin SOIC / WLCSP	SAM D10C – 14-pin SOIC
Pins	24	20	14
General Purpose I/O-pins (GPIOs)	22	18	12
Flash	16/8KB	16/8KB	16/8KB
SRAM	4KB	4KB	4KB
Timer Counter (TC)	2	2	2 ⁽³⁾
Waveform output channels for TC	2	2	2
Timer Counter for Control (TCC)	1	1	1
Waveform output channels per TCC	8	8	8
DMA channels	6	6	6
Serial Communication Interface (SERCOM)	3	3	2
Analog-to-Digital Converter (ADC) channels	10	8	5
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1

Table 1-1. Configuration Summary (Continued)

	SAM D10D – 24-pin QFN	SAM D10D – 20-pin SOIC / WLCSP	SAM D10C – 14-pin SOIC
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	8	8	8
Peripheral Touch Controller (PTC) channels (X- x Y-lines) for mutual capacitance ⁽¹⁾	72 (9x8)	42 (7x6)	12 (4x3)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-lines only) ⁽²⁾	16	13	7
Maximum CPU frequency	48MHz	48MHz	48MHz
Packages	QFN	SOIC / WLCSP	SOIC
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	6	6	6
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

- Notes:
1. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number in the [“Configuration Summary” on page 3](#) is the maximum number of channels that can be obtained.
 2. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.
 3. The signals for TC2 are not routed out on the 14-pin package.

2. Ordering Information



2.1 SAM D10C – 14-pin SOIC

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10C13A-SSUT	8K	4K	SOIC14	Tape & Reel
ATSAMD10C13A-SSNT	8K	4K	SOIC14	Tape & Reel
ATSAMD10C14A-SSUT	16K	4K	SOIC14	Tape & Reel
ATSAMD10C14A-SSNT	16K	4K	SOIC14	Tape & Reel

2.2 SAM D10D – 20-pin SOIC

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D13A-SSUT	8K	4K	SOIC20	Tape & Reel
ATSAMD10D13A-SSNT	8K	4K	SOIC20	Tape & Reel
ATSAMD10D14A-SSUT	16K	4K	SOIC20	Tape & Reel
ATSAMD10D14A-SSNT	16K	4K	SOIC20	Tape & Reel

2.3 SAM D10D – 20-ball WLCSP

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D14A-UUT	16K	4K	WLCSP20	Tape & Reel

2.4 SAM D10D – 24-pin QFN

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD10D13A-MUT	8K	4K	QFN24	Tape & Reel
ATSAMD10D13A-MNT	8K	4K	QFN24	Tape & Reel
ATSAMD10D14A-MUT	16K	4K	QFN24	Tape & Reel
ATSAMD10D14A-MNT	16K	4K	QFN24	Tape & Reel

2.5 Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 2-1. Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD10D14AM	0x00	0x10020r00
SAMD10D13AM	0x01	0x10020r01
Reserved	0x02	
SAMD10D14ASS	0x03	0x10020r03
SAMD10D13ASS	0x04	0x10020r04
Reserved	0x05	
SAMD10C14A	0x06	0x10020r06
SAMD10C13A	0x07	0x10020r07
Reserved	0x08	
SAMD10D14AU	0x09	0x10020r09

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die